

SHB Express: The next big thing in passive backplanes and slot boards



By *Jim Renahan*

Did you know that the origins of PICMG began with several companies coming together to develop the first open standard for industrial computers using slot boards and passive backplanes? The industry standard that resulted from this initial specification effort was called PICMG 1.0, which set the stage for many new and exciting developments in passive backplane and slot board technology.

As new technologies and standards evolved, the terms *passive backplanes* and *slot boards* came to mean different things to different people. For our purposes, we will restrict the use of the term *slot board* to describe Single Board Computers (SBCs) or System Host Boards (SHBs) that use edge connectors to plug into backplanes (passive or otherwise) used in PICMG 1.3 or SHB Express systems. In this article we'll focus on SHB Express systems and discuss applications, market size, and the technology differences of PICMG 1.0, 1.2, and 1.3 (PICMG 1.x) slot board SBCs/SHBs and backplanes.

Slot board SBCs and backplanes cover a broad range of applications in diverse markets such as military/aerospace, industrial automation, communications, medical, and instrumentation. The major advantage of PICMG 1.x SBCs and backplanes is that these systems effectively support multiple option board slots (PCI Express, PCI-X, PCI, and ISA), fast Mean Time To Repair (MTTR) and flexible backplane slot configurations. One of the distinct advantages offered by PICMG 1.x systems is the ability to take advantage of the plethora of commercially available off-the-shelf plug-in option boards. Choices abound in the types of option boards available to meet various system design requirements. The numbers and choices of option boards available in the slot board form factor will keep PICMG 1.x system implementation options viable for the foreseeable future. Figure 1 illustrates a "typical" chassis populated with a PICMG 1.3 system host board and a

backplane with PCI Express, PCI-X, and PCI option board slots.

The slot board SBC and passive backplane market is a diverse and constantly evolving market. You may find that surprising given all the attention focused on newer PICMG 2.x and PICMG 3.x technologies. That's understandable because it's easy to get excited about new specifications and markets, and bypass the tried and true technologies represented by PICMG 1.x.

Several market studies state that growth for PICMG 1.x products has remained steady and should continue that way over the next several years. Figure 2 illustrates a respectable growth rate for PICMG 1.x products from 2004 through 2008. In the base year of 2004, total US market shipments for PICMG 1.x SBC/SHBs and backplanes were likely around the \$218 million mark, with 2008 shipments estimated to grow to \$270 million. Granted this isn't the "billions and billions" of

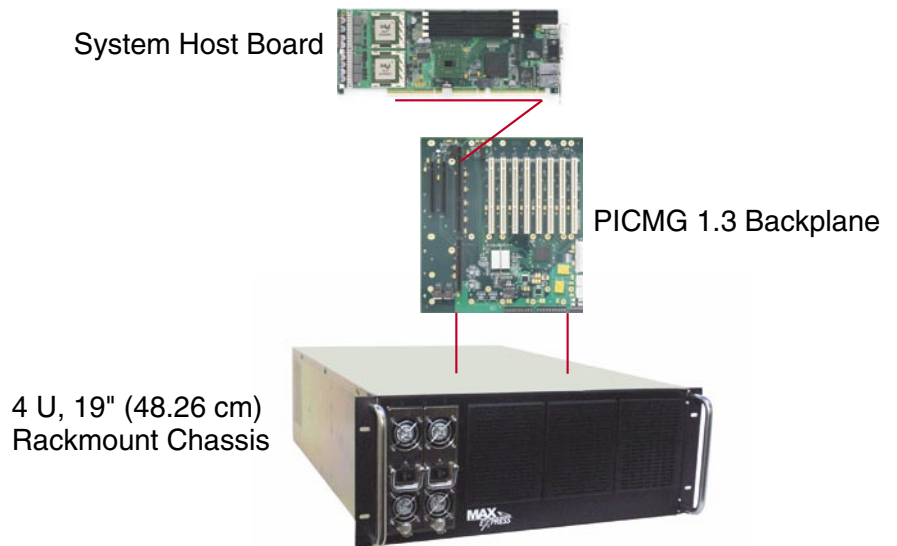


Figure 1

PICMG 1.x Slot SBC/SHBs and Backplanes Market Shipments

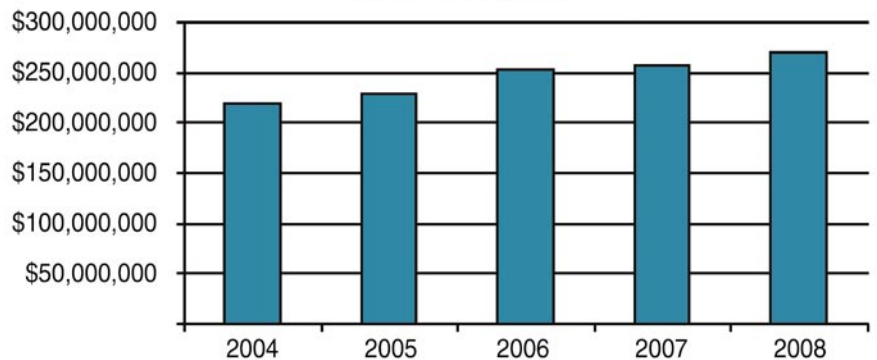


Figure 2

dollars associated with other technology markets, but these are “real” numbers based on years of shipping data and market observations. When comparing board-only shipping data, PICMG 1.x products represent a respectable portion of 2004 embedded computing shipments.

SHB Express/PICMG 1.3 represents the latest innovation in the PICMG 1.x market. SHB Express is a new industry standard, recently adopted by the PICMG membership, and replaces the PCI/ISA, PCI-X parallel bus single board computer-to-backplane interfaces used in PICMG 1.0 and 1.2 with PCI Express serial interconnects. Figure 3 shows the evolution of PICMG 1.x slot board to backplane interconnects.



PCI/ISA Interfaces - PICMG 1.0



PCI-X/PCI-X Interfaces - PICMG 1.2



PCI Express Interfaces - PICMG 1.3

Figure 3

With the speed of today’s processors and chipsets the data bottlenecks tend to be moving out to the peripheral I/O. The PICMG 1.0 standard defines PCI/ISA parallel bus interconnects between the single board computer and backplane. PICMG 1.2 increased the data throughput speed between the SBC and backplane by replacing the ISA parallel bus with the PCI-X parallel bus. This helped the data bottleneck issue a little bit but did not address the root cause of the problem: parallel bus technology. PICMG 1.3 addresses the inherent limitation of parallel bus technology by replacing the PCI/ISA and PCI-X/PCI-X interfaces with multiple, scalable, full-duplex, PCI Express links between the system host board and the backplane. The term SHB was used in developing the PICMG 1.3

specification in order to make a clean break between the parallel bus technology of PICMG 1.0 and the scalable serial interface technology offered by PICMG 1.3. Functionally speaking the SBC and SHB accomplish the same basic tasks in their respective PICMG 1.0, 1.2, and PICMG 1.3 systems. Often the terms SHB and SBC are used interchangeably. Figure 4 compares the peak available bandwidth capabilities of PCI/PCI-X parallel bus interfaces and PCI Express (Gen. 1).

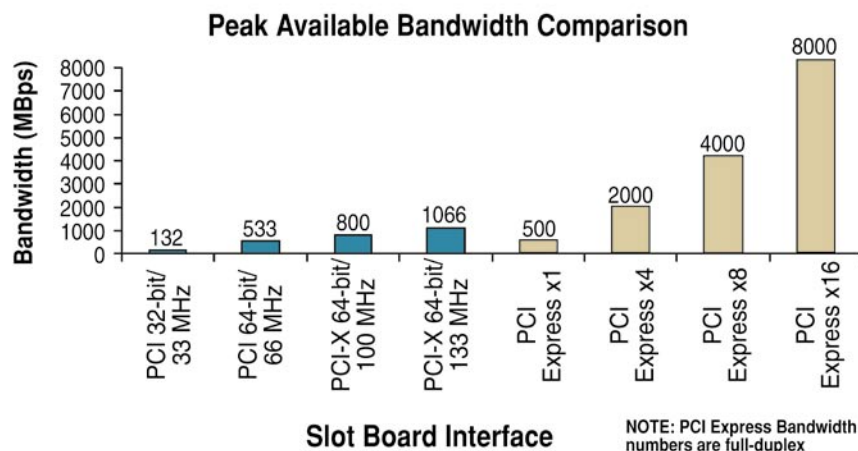


Figure 4

The PICMG 1.3 specification defines some interesting features that can be implemented by the compatible SHBs and backplanes. Optional I/O can be routed through the SHB’s edge connector C and down to the backplane in order to decrease MTTR by moving some cable connections from the SHB down to the backplane. The optional I/O capabilities defined in the specification include:

- Four USB
- Dual SATA
- Dual 10/100/1000BASE-T Ethernet

Soft power control implementations in PICMG 1.0 and 1.2 systems were always a bit tricky. SHB Express addresses this inherent limitation by defining Advanced Configuration and Power Interface (ACPI) functionality support in the specification. An SHB Express system can support various soft power control/wake states associated with the ACPI control signals.

The SHB Express specification also defines Intelligent Platform Management Interface (IPMI) and Geographic Addressing (GA) signal placements on the SHB’s edge connector. These signals could be utilized in a PICMG 1.3 system to implement advanced system functions like IPMI and Hot Swap in a slot board

and passive backplane system. This represents a future capability since today’s slot boards do not typically support IPMI and GA. Typically, this functionality has been restricted to AdvancedTCA systems, but SHB Express puts the “hooks” in place to support this key system capability in the PICMG 1.3 form factor.

One of the design advantages of PCI Express is that far fewer signal pins are required than older ISA/PCI/PCI-X par-

allel interfaces. This allows us to provide additional edge connector contacts for SHB power and signal grounds. The net result is that we can have the +12 V auxiliary power cable(s) plug into the PICMG 1.3 backplane and route the power signals and grounds over to the SHB edge connector slot. This new capability simplifies the power cable connections and helps decrease MTTR by moving the power connectors off the SHB and down to the backplane.

The SHB Express specification is very flexible in terms of PCI Express implementations. The specification allows for up to 20 PCI Express links between the SHB and backplane. These links can be configured in a variety of different ways. The number and type of PCI Express links routed from the SHB to the backplane is largely dependent on the type of chipset used on the SHB.

Graphics class and server class

SHB Express system host boards and backplanes fall into two broad categories: Graphics Class and Server Class. A graphics-class SHB has one x16 and either one x4 or four x1 PCI Express electrical connections to the backplane. Graphics-class backplanes have one PCI Express option board slot “plumbed” with a x16 electri-

cal interface and several x1 board slots or one x4 slot.

Server-class SHBs and backplanes are designed to maximize the number of high-bandwidth PCI Express connections. A typical server-class SHB may have a combination of x8 and x4 links routed to the backplane. The PCI Express board slots on a server-class backplane are electrically configured as x8 or x4 slots.

The PCI Express option board slots on any PICMG 1.3 backplane may mechanically support boards with interfaces greater than that which is electrically supported. In most cases, PCI Express's auto-negotiation capability will automatically establish communication between the SHB and the option board. Link configuration straps between the PCI Express backplane board slots and the SHB are defined in the specification for system host board

designs that may not support the auto-negotiation capability.

With available bridge technology, SHB Express backplanes and SHBs support PCI Express, PCI-X, and PCI option boards. Believe it or not, there is still a demand to support ISA slots on the backplane, which can be accomplished with the use of PCI-to-ISA bridge technology. However, the cost justification of migrating an older board technology to a newer technology can be prohibitive. Figure 5 shows two examples of PICMG 1.3 backplane designs.

Conclusion

The only sure bet in the world of technology is change, and the SHB Express specification is built to support this reality. The PCI Express technology that you can purchase on the open market today supports the Gen 1 implementation of PCI Express

with its signal frequency of 2.5 gigabits per second (Gbps) per lane and per direction. Option boards and chipsets will soon be available with PCI Express Gen 2 with double the signaling frequency. Advanced Switching adds additional functionality to the PCI Express protocol layers to enable advanced fabric network capability. When developing the SHB Express specification, the PICMG 1.3 Technical Subcommittee took these upcoming technology advancements into consideration. As a result, SHB Express supports both current and future iterations of PCI Express technology, including Advanced Switching. The good news is that SHB Express products support past, present, and future slot board technologies while enabling a seamless and cost-effective transition to PCI Express and Advanced Switching.

Graphics-Class PICMG 1.3 Backplanes

Server-Class PICMG1.3 Backplanes

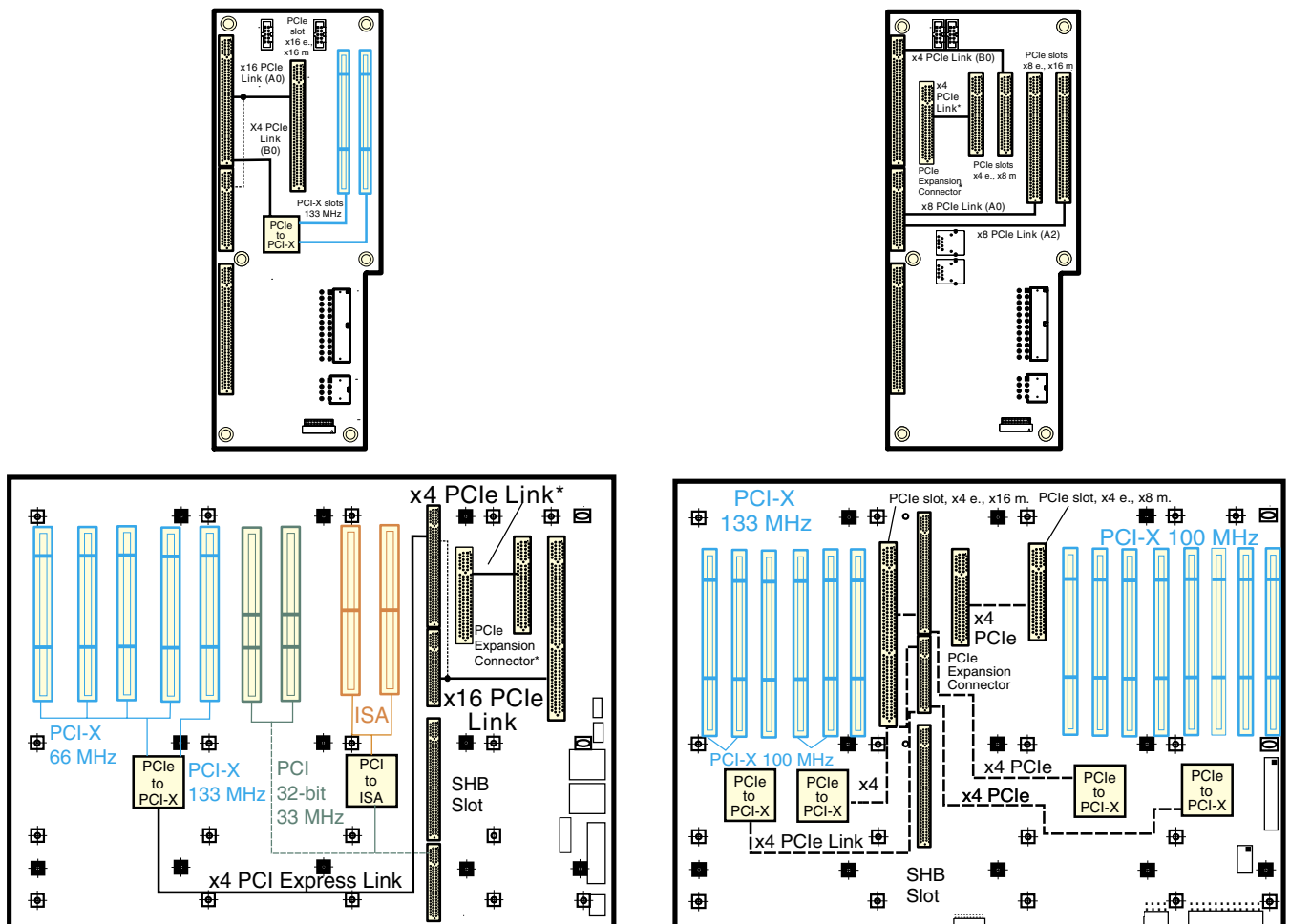


Figure 5

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