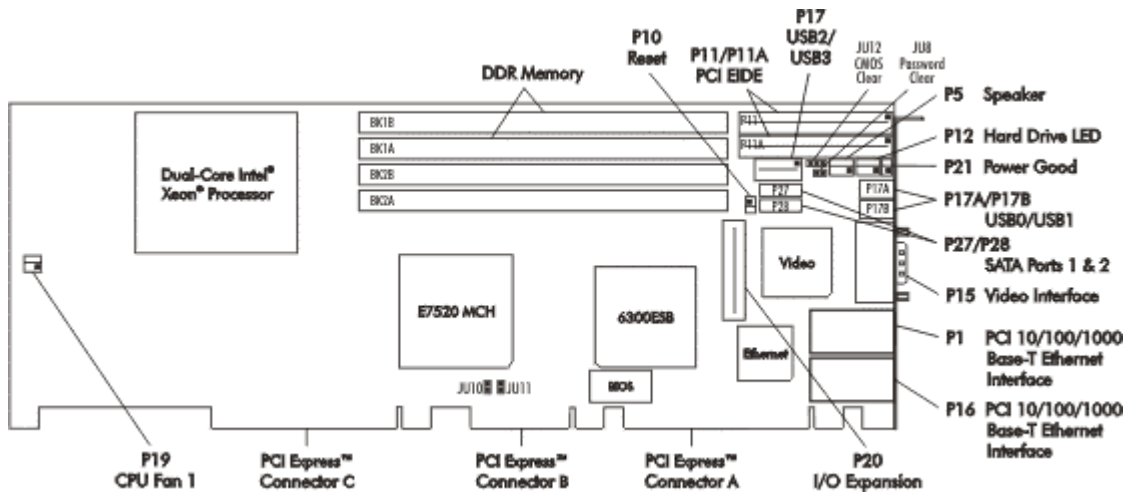




Technical Information – Jumpers, Connectors and Memory SLI (6521-xxx) System Host Board

Layout Diagram



Jumpers & LEDs

The setup of the configuration jumpers on the SHB is described below. An asterisk (*) indicates the default value of each jumper.

NOTE: For two-position jumpers (3-post), "RIGHT" is toward the bracket end of the board; "LEFT" is toward the processor.

JU8 Password Clear

Install for one power-up cycle to reset the password to the default (null password).
 Remove for normal operation. *

JU10/11 System Flash ROM Operational Modes

The Flash ROM has two programmable sections: the Boot Block for "flashing" in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system.

| | JU10 | JU11 |
|----------------------------|----------|----------|
| All Blocks Write Enabled | Remove * | Remove * |
| Boot Block Write Protected | Install | Remove |
| Block 2-16 Write Protected | Remove | Install |

JU12 CMOS Clear

Install on the LEFT to operate. *
 Install on the RIGHT to clear.

NOTE: To clear the CMOS, power down the system and install the jumper on the RIGHT. Wait for at least two seconds, move the jumper back to the LEFT and turn the power on. When AMIBIOS displays the "CMOS Settings Wrong" message, press F1 to go into the BIOS Setup Utility, where you may reenter your desired BIOS settings, load optimal defaults or load failsafe defaults.



Jumpers & LEDs (continued)

Ethernet LEDs

Each Ethernet interface has two LEDs for status indication and an RJ-45 network connector.

| LED/Connector | Description |
|--------------------------|---|
| Activity LED | Orange LED which indicates network activity. This is the upper LED on the LAN connector (i.e., toward the memory sockets). |
| Off | No current network transmit or receive activity |
| On (flashing) | Indicates network transmit or receive activity. |
| Speed LED | Bi-color (green/orange) LED which identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors). |
| Green | Indicates a valid link at 1000-Mb/s |
| Orange | Indicates a valid link at 100-Mb/s |
| Off | Indicates a valid link at 10-Mb/s |
| RJ-45 Network Connectors | The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection. |

ACPI Status LED

The ACPI status LED (LED9), which is located to the right of the CPU fan, indicates the power level of the SHB, as shown below:

| LED Status | Description |
|-------------------|--|
| Off | Indicates that the SHB is running at full power. |
| On | Indicates that the SHB is in S3, S4 or S5 sleep state. |

POST Code LEDs

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0 through 7, which are located below the memory banks and are numbered from right (0) to left (7). Refer to the board layouts earlier in this chapter for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. Specific error codes are listed in Appendix A - BIOS Messages section of the SLI Technical Reference Manual, along with a chart to interpret the LEDs into hexadecimal format.

CPU Throttling LED

The CPU throttling LED (LED8), which is located to the right of the memory banks, indicates the status of CPU thermal shutdown, as shown below:

| LED Status | Description |
|-------------------|--|
| Off | Indicates the CPU is operating within acceptable thermal levels. |
| On (flashing) | Indicates the CPU is throttling down to a lower operating speed due to rising CPU temperature. |
| On (solid) | Indicates the CPU has reached the thermal shutdown threshold limit. The SHB is still operating, but a thermal shutdown may soon occur. |



NOTE: When a thermal shutdown occurs, the LED will stay on in systems using non- ATX/EPS power supplies. The CPU will cease functioning, but power will still be applied to the SHB. In systems with ATX/EPS power supplies, the LED will turn off when a thermal shutdown occurs because system power is removed via the ACPI soft control power signal S5. In this case, all SHB LEDs will turn off; however, stand-by power will still be present.

Jumpers & LEDs (continued)

CPU Throttling LED

The CPU throttling LED (LED9), which is located in the upper left corner of the SLI, indicates the status of CPU thermal shutdown, as shown below:

| LED Status | Description |
|-------------------|--|
| Off | Indicates the CPU is operating within acceptable thermal levels. |
| On (flashing) | Indicates the CPU is throttling down to a lower operating speed due to rising CPU temperature. |
| On (solid) | Indicates the CPU has reached the thermal shutdown threshold limit. The SHB is still operating, but a thermal shutdown may soon occur. |

NOTE: When a thermal shutdown occurs, the LED will stay on in systems using non- ATX/EPS power supplies. The CPU will cease functioning, but power will still be applied to the SHB. In systems with ATX/EPS power supplies, the LED will turn off when a thermal shutdown occurs because system power is removed via the ACPI soft control power signal S5. In this case, all SHB LEDs will turn off; however, stand-by power will still be present.



Connectors

NOTE:

Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - 10/100/1000Base-T Ethernet Connectors - LAN2

Dual RJ-45 connector, Belfuse #0826-1X1T-23

PIN SIGNAL

| | |
|---|-------|
| 1 | TRP1+ |
| 2 | TRP1- |
| 3 | TRP2+ |
| 4 | TRP3+ |
| 5 | TRP3- |
| 6 | TRP2- |
| 7 | TRP4+ |
| 8 | TRP4- |

P5 - SPEAKER PORT CONNECTOR

4 pin single row header, Amp #640456-4

PIN SIGNAL

| | |
|---|--------------|
| 1 | Speaker Data |
| 2 | Key |
| 3 | Gnd |
| 4 | +5V |

P7 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0821
 (+5V fused with self-resetting fuses)

| PIN | SIGNAL | PIN | SIGNAL |
|------------|---------------|------------|---------------|
| 1 | +5V - USB2 | 2 | +5V - USB3 |
| 3 | USB2- | 4 | USB3- |
| 5 | USB2+ | 6 | USB3+ |
| 7 | Gnd - USB2 | 8 | Gnd - USB3 |
| 9 | Chassis Gnd | 10 | Chassis Gnd |

P16 - 10/100/1000Base-T Ethernet Connectors - LAN1

Dual RJ-45 connector, Belfuse #0826-1X1T-23

PIN SIGNAL

| | |
|---|-------|
| 1 | TRP1+ |
| 2 | TRP1- |
| 3 | TRP2+ |
| 4 | TRP3+ |
| 5 | TRP3- |
| 6 | TRP2- |
| 7 | TRP4+ |
| 8 | TRP4- |

P17A - UNIVERSAL SERIAL BUS (USB) CONNECTOR

USB vertical connector, Molex #67-329-0000
 (+5V fused with self-resetting fuse)

PIN SIGNAL

| | |
|---|------------|
| 1 | +5V - USB0 |
| 2 | USB0- |
| 3 | USB0+ |
| 4 | Gnd - USB0 |

P17B - UNIVERSAL SERIAL BUS (USB) CONNECTOR

USB vertical connector, Molex #67-329-0000
 (+5V fused with self-resetting fuse)

PIN SIGNAL

| | |
|---|------------|
| 1 | +5V - USB1 |
| 2 | USB1- |
| 3 | USB1+ |
| 4 | Gnd - USB1 |



Connectors (Continued)

P10 - External Reset Connector

2 pin single row header, Amp #640456-2

| PIN | SIGNAL |
|-----|--------------------------------|
| 1 | External Reset In (Low Active) |
| 2 | Gnd |

P11 - Primary IDE Hard Drive Connector

40 pin dual row header, 3M #30340-6002HB

| PIN | SIGNAL | PIN | SIGNAL |
|-----|---------|-----|-----------|
| 1 | Reset | 2 | Gnd |
| 3 | Data 7 | 4 | Data 8 |
| 5 | Data 6 | 6 | Data 9 |
| 7 | Data 5 | 8 | Data 10 |
| 9 | Data 4 | 10 | Data 11 |
| 11 | Data 3 | 12 | Data 12 |
| 13 | Data 2 | 14 | Data 13 |
| 15 | Data 1 | 16 | Data 14 |
| 17 | Data 0 | 18 | Data 15 |
| 19 | Gnd | 20 | NC |
| 21 | DRQ 0 | 22 | Gnd |
| 23 | IOW | 24 | Gnd |
| 25 | IOR | 26 | Gnd |
| 27 | IORDY | 28 | SELPDP |
| 29 | DACK 0 | 30 | Gnd |
| 31 | IRQ 14 | 32 | NC |
| 33 | Add 1 | 34 | PCBL DET* |
| 35 | Add 0 | 36 | Add 2 |
| 37 | CS 1P | 38 | CS 3P |
| 39 | IDEACTP | 40 | Gnd |

P19 - CPU FAN

3 pin single row header, Molex #22-23-2031

| PIN | SIGNAL |
|-----|----------|
| 1 | Gnd |
| 2 | +12V |
| 3 | Fan Tach |

P20 - I/O Expansion Mezzanine Card Connector

76 pin controlled impedance connector,
 Samtec #MIS-038-01-FD-K

| PIN | SIGNAL | PIN | SIGNAL |
|-----|----------------|-----|-------------|
| 1 | +12V | 2 | +5V_STANDBY |
| 3 | NC | 4 | +5V_STANDBY |
| 5 | NC | 6 | +5V_DUAL |
| 7 | NC | 8 | +5V_DUAL |
| 9 | NC | 10 | NC |
| 11 | NC | 12 | NC |
| 13 | ICH_SMI# | 14 | ICH_RCIN# |
| 15 | ICH_SIOPME# | 16 | ICH_A20GATE |
| 17 | Gnd | 18 | Gnd |
| 19 | L_FRAME# | 20 | L_AD3 |
| 21 | L_DRQ1# | 22 | L_AD2 |
| 23 | L_DRQ0# | 24 | L_AD1 |
| 25 | SERIRQ | 26 | L_AD0 |
| 27 | Gnd | 28 | Gnd |
| 29 | PCLK14SIO | 30 | PCLK33LPC |
| 31 | Gnd | 32 | Gnd |
| 33 | SMBDATA_RESUME | 34 | IPMB_DAT |
| 35 | SMBCLK_RESUME | 36 | IPMB_CLK |
| 37 | SALRT#_RESUME | 38 | IPMB_ALRT# |
| 39 | Gnd | 40 | Gnd |
| 41 | EXP_CLK100 | 42 | EXP_RESET# |
| 43 | EXP_CLK100# | 44 | ICH_WAKE# |
| 45 | Gnd | 46 | Gnd |
| 47 | C_PE_TXP4 | 48 | C_PE_RXP4 |
| 49 | C_PE_TXN4 | 50 | C_PE_RXN4 |



Connectors (Continued)

P11A - Secondary IDE Hard Drive Connector
 40 pin dual row header, 3M #30340-6002HB

| PIN | SIGNAL | PIN | SIGNAL |
|-----|---------|-----|-----------|
| 1 | Reset | 2 | Gnd |
| 3 | Data 7 | 4 | Data 8 |
| 5 | Data 6 | 6 | Data 9 |
| 7 | Data 5 | 8 | Data 10 |
| 9 | Data 4 | 10 | Data 11 |
| 11 | Data 3 | 12 | Data 12 |
| 13 | Data 2 | 14 | Data 13 |
| 15 | Data 1 | 16 | Data 14 |
| 17 | Data 0 | 18 | Data 15 |
| 19 | Gnd | 20 | NC |
| 21 | DRQ 1 | 22 | Gnd |
| 23 | IOW | 24 | Gnd |
| 25 | IOR | 26 | Gnd |
| 27 | IORDY | 28 | SELPDS |
| 29 | DACK 1 | 30 | Gnd |
| 31 | IRQ 15 | 32 | NC |
| 33 | Add 1 | 34 | SCBL DET* |
| 35 | Add 0 | 36 | Add 2 |
| 37 | CS 1S | 38 | CS 3S |
| 39 | IDEACTS | 40 | Gnd |

| | | | |
|----|-----------|----|-----------|
| 51 | Gnd | 52 | Gnd |
| 53 | C_PE_TXP3 | 54 | C_PE_RXP3 |
| 55 | C_PE_TXN3 | 56 | C_PE_RXN3 |
| 57 | Gnd | 58 | Gnd |
| 59 | C_PE_TXP2 | 60 | C_PE_RXP2 |
| 61 | C_PE_TXN2 | 62 | C_PE_RXN2 |
| 63 | Gnd | 64 | Gnd |
| 65 | C_PE_TXP1 | 66 | C_PE_RXP1 |
| 67 | C_PE_TXN1 | 68 | C_PE_RXN1 |
| 69 | Gnd | 70 | Gnd |
| 71 | +3.3V | 72 | +5V |
| 73 | +3.3V | 74 | +5V |
| 75 | +3.3V | 76 | +5V |

P21 - POWER GOOD LED

2 pin single row header, Amp #640456-2

| PIN | SIGNAL |
|-----|--------|
| 1 | LED - |
| 2 | LED + |

P27 - SATA PORT1

7 pin vertical connector, Molex #67491-0031

| PIN | SIGNAL | PIN | SIGNAL |
|-----|--------|-----|--------|
| 1 | Gnd | 5 | RX- |
| 2 | TX+ | 6 | RX+ |
| 3 | TX- | 7 | Gnd |
| 4 | Gnd | | |

P28 - SATA PORT2

7 pin vertical connector, Molex #67491-0031

| PIN | SIGNAL | PIN | SIGNAL |
|-----|--------|-----|--------|
| 1 | Gnd | 5 | RX- |
| 2 | TX+ | 6 | RX+ |
| 3 | TX- | 7 | Gnd |
| 4 | Gnd | | |

* For ATA/66 and ATA/100 drives, which should be set for Cable Select for proper speed operation. If other Drives are detected, pin definition is Gnd.

P12 - HARD DRIVE LED CONNECTOR

4 pin single row header, Amp #640456-4

| PIN | SIGNAL |
|-----|--------|
| 1 | LED + |
| 2 | LED - |



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3 LED -

4 LED +

Connectors (Continued)

P15 - VIDEO INTERFACE CONNECTOR

15 pin HD15 connector, Amp #1-1470250-3

| PIN | SIGNAL | PIN | SIGNAL | PIN | SIGNAL |
|------------|---------------|------------|---------------|------------|---------------|
| 1 | Red | 6 | Gnd | 11 | NC |
| 2 | Green | 7 | Gnd | 12 | EEDI |
| 3 | Blue | 8 | Gnd | 13 | HSYNC |
| 4 | NC | 9 | +5V | 14 | VSYNC |
| 5 | Gnd | 10 | Gnd | 15 | EECS |



Memory

The Double Data Rate 2 (DDR2) memory interface supports up to 8GB of memory and can operate as either a single-channel or dual-channel interface. Each of the channels (A and B) terminates in two dual in-line memory module (DIMM) sockets. The System BIOS automatically detects memory type, size and speed.

The SHB uses industry standard 72-bit wide ECC gold finger memory modules in four 240-pin sockets. The DIMMs must be PC2-3200 compliant and have the following features:

- 240-pin with gold-plated contacts
- ECC (72-bit) DDR2 memory
- Dual rank or single rank DIMMs
- Registered configuration

The following DIMM sizes are supported:

| DIMM Size | DIMM Type | ECC |
|-----------|------------|-----------|
| 256 MB | Registered | 32M x 72 |
| 512 MB | Registered | 64M x 72 |
| 1 GB | Registered | 128M x 72 |
| 2 GB | Registered | 256M x 72 |

NOTE: With the bracket end of the board to the right, the DIMM sockets are numbered 1B, 1A, 2B and 2A, from top to bottom. All memory modules must have gold contacts.

Populating identical DIMMs in pairs (one each in the A and B channels) results in dual-channel operation. In dual-channel mode, the DIMM pair operates in lockstep, theoretically doubling the memory bandwidth.

When a single DIMM is used, it should be installed in DIMM socket 1B. With this configuration, the interface operates as a single-channel interface with a theoretical memory bandwidth of 3.2GB/s.

Installing two DIMMs which are identical in type, size and rank in DIMM sockets 1B and 1A results in dual-channel operation, which doubles the theoretical memory interface bandwidth to 6.4GB/s. Installing additional DIMMs in sockets 2B and 2A also results in the higher bandwidth. In this case, the DIMMs installed in sockets 2B and 2A must be identical in type, size and rank to each other, but may be different in size from the pair installed in sockets 1B and 1A. If the modules in channel B and channel A (e.g., 1B and 1A) differ in size, the BIOS will use the size of the smallest DIMM.

Installing DIMMs only in sockets 1B and 2B results in single-channel mode, since both DIMMs are in the B channel. If the DIMMs are identical in type and size, they should be populated in sockets 1B and 1A to operate in dual-channel mode.

NOTE: The SLI supports a DDR2-400 memory interface speed. If modules of higher speeds are used, they will clock down to a DDR2-400 memory interface speed.

DDR2 memory modules are available as either single rank or dual rank DIMMs. A rank refers to the 72-bit unit of devices or DRAM chips that make up the PC2-3200 ECC registered 240-pin DDR2 DIMM. Single or dual rank memory modules must be placed in the SHB's DIMM sockets using prescribed population rules to ensure proper memory interface operation and performance.



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The following table explains the DDR2 DIMM population rules:

| | DIMM Socket | | | |
|----------------------------|-----------------------|-------------|-------------|-------------|
| | 1B (top-most DIMM) | 1A | 2B | 2A |
| 1 Single Rank | Single Rank | Empty | Empty | Empty |
| 1 Dual Rank | Dual Rank | Empty | Empty | Empty |
| 2 Single Rank | Single Rank | Single Rank | Empty | Empty |
| 1 Dual Rank, 1 Single Rank | Dual Rank | Single Rank | Empty | Empty |
| 2 Dual Rank | Dual Rank | Dual Rank | Empty | Empty |
| 3 Single Rank | Single Rank | Single Rank | Single Rank | Empty |
| 1 Dual Rank, 2 Single Rank | Dual Rank | Single Rank | Single Rank | Empty |
| 4 Single Rank | Single Rank | Single Rank | Single Rank | Single Rank |

[SLI Product Detail.](#)